



Teradyne Tiger

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# Confsim file created on: 11/07/07 08:56:10 # # Tiger tester
# # is a 2 processor system
# Processor 1: 1280 MHz sparcv9 (online)
# Processor 2: 1280 MHz sparcv9 (online)
# PCI based system
# Terabus is present
# Board ID
# Serial number
# TCI is present
#
```

```
TIGER_TH 1
BACKPLANE A
#Slot Type Num XptA XptB Name
2 949-658-60 0 # 23 24 LFAC DUAL CC
3 000-000-00 0 # 21 22 EMPTY
4 949-658-60 0 # 19 20 LFAC DUAL CC
5 879-906-61 0 # 17 18 VHFCW CC
6 949-658-60 0 # 15 16 LFAC DUAL CC
7 000-000-00 0 # 13 14 EMPTY
8 949-831-60 0 # 11 12 1G VHFD CC
9 949-818-60 0 # 9 10 VHFAWG2500 CC
10 949-831-60 0 # 7 8 1G VHFD CC
11 949-818-60 0 # 5 6 VHFAWG2500 CC
14 949-831-60 0 # 25 26 1G VHFD CC
15 949-818-60 0 # 27 28 VHFAWG2500 CC
16 949-831-60 0 # 29 30 1G VHFD CC
17 949-818-60 0 # 31 32 VHFAWG2500 CC
18 939-227-60 0 # 33 34 GIGADIG CC
19 000-000-00 0 # 35 36 EMPTY
20 000-000-00 0 # 37 38 EMPTY
21 879-906-61 0 # 39 40 VHFCW CC
22 949-894-00 0 # 41 42 QVS CC
23 000-000-00 0 # 43 44 EMPTY
1 949-886-00 0 # 3 0 ACISB-L
24 949-886-01 0 # 4 0 ACISB-R
END
```

```
#
# Up to 4 Precision AC Card Cages are allowed # PRECISION_AC 1
#Slot Type Num Name
1 949-664-00 0 # VHFDIG MF
2 949-819-00 0 # VHFAWG2500
3 949-664-00 0 # VHFDIG MF
4 949-819-00 0 # VHFAWG2500
5 949-660-01 0 # LFACDIG
6 949-659-00 0 # LFACSRC
7 949-861-00 0 # TJA BOARD
8 949-671-20 0 # PACS CAGE INT
END
```

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Teradyne Tiger (continued)

PRECISION_AC 2

#Slot	Type	Num	Name
1	949-660-01	0	# LFACDIG
2	949-659-00	0	# LFACSRC
3	949-659-00	0	# LFACSRC
4	000-000-00	0	# EMPTY
5	000-000-00	0	# EMPTY
6	949-664-00	0	# VHFDIG MF
7	949-819-00	0	# VHFAWG2500
8	949-671-20	0	# PACS CAGE INT

END

PRECISION_AC 3

#Slot	Type	Num	Name
1	000-000-00	0	# EMPTY
2	000-000-00	0	# EMPTY
3	949-664-00	0	# VHFDIG MF
4	949-819-00	0	# VHFAWG2500
5	949-664-20	0	# GIGADIG MF
6	000-000-00	0	# EMPTY
7	000-000-00	0	# EMPTY
8	949-671-20	0	# PACS CAGE INT

END

 # Up to 8 Universal Backplane/Synch Power Subsystem # cages are allowed # # For the Synch
 Power Subsystem:
 # Slot Type Name Instr1 # Instr2 # Ammeter #
 #
 # Instr1 # - instrument connected to the first two matrix lines
 # Instr2 # - instrument connected to the last two matrix lines
 # Ammeter # - ammeter connection
 # to AVOID errors, put NO 0 if no instrument is connected.
 #

UB_SPS_CAGE 1

# Slot	Type	Num	Name
1	879-802-02	0	# UB_SPS_802
2	517-301-00	0	# UB_APU
3	517-301-00	0	# UB_APU
4	517-301-00	0	# UB_APU
5	517-301-00	0	# UB_APU
6	517-301-00	0	# UB_APU
7	517-301-00	0	# UB_APU
8	517-301-00	0	# UB_APU
9	517-301-00	0	# UB_APU
10	517-301-00	0	# UB_APU
11	517-301-00	0	# UB_APU
12	517-301-00	0	# UB_APU
13	517-301-00	0	# UB_APU
14	879-925-01	0	# UB_60_V_SRC MAT 1
15	879-925-01	0	# UB_60_V_SRC MAT 3
16	879-925-01	0	# UB_60_V_SRC DUT 1
17	879-925-01	0	# UB_60_V_SRC DUT 5
18	879-925-01	0	# UB_60_V_SRC DUT 6
19	879-925-01	0	# UB_60_V_SRC DUT 7
20	879-925-01	0	# UB_60_V_SRC DUT 8
21	879-690-00	0	# UB_ASY
22	517-300-01	0	# UB_TJ300

END

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```
UB_SPS_CAGE 2
# Slot Type Num Name
  1 879-802-02 0 # UB_SPS_802
  4 949-700-10 0 # UB_QVS_CAL 1
  5 949-693-10 0 # UB_QVS_CTRL 22 ??
  6 949-698-10 0 # UB_QVS_AM 1
  7 949-698-10 0 # UB_QVS_AM 2
 22 517-300-01 0 # UB_TJ300
END

CSB_CAGE 8
#Slot Type Num Fld1 Fld2 Name
  1 949-920-60 0 # HSD CSB
  2 949-866-00 0 # SPLITTER
END

TIGER_TH 1
BACKPLANE B
#Slot Type Num Name
 30 805-873-50 0 # QSB
 34 805-870-70 0 # PE32 128M
 35 805-902-02 0 # DPE32 128M
 36 805-870-70 0 # PE32 128M
 37 805-902-02 0 # DPE32 128M
 38 805-870-70 0 # PE32 128M
 39 805-873-03 0 # QSB HCLK
 40 805-870-70 0 # PE32 128M
 41 805-902-02 0 # DPE32 128M
 42 805-870-70 0 # PE32 128M
 43 805-902-02 0 # DPE32 128M
 45 805-902-02 0 # DPE32 128M
 46 805-902-02 0 # DPE32 128M
 47 805-870-70 0 # PE32 128M
 48 805-870-70 0 # PE32 128M
 49 805-873-03 0 # QSB HCLK
 50 805-902-02 0 # DPE32 128M
 51 805-870-70 0 # PE32 128M
 52 805-870-70 0 # PE32 128M
 53 805-902-02 0 # DPE32 128M
 58 805-873-50 0 # QSB
END

#
# Time Subsystem
#
TIME_SUBSYSTEM
# Board ID # Name
 949-782-00 # Time Mux Board 1
 949-782-00 # Time Mux Board 2 END
```

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```

#
# DC Subsystem -
#
#   SRC <NUM>                [1 - 13]
#   (sources 1-5 are MATRIX sources 1-5
#   sources 6-13 are DUT sources 1-8)
#   HCU <NUM>                 *[1 - 4]
#   REF HCU <NUM>             *[1 - 4]
#   HVSRC <NUM>               *[1 - 4]
#   PWSRC <NUM>               [1 - 4]
#   DATABITS <NUM> - <NUM>    [1 - 192]
#
# ** These instruments share the same seven-slot cage -- only one
# instrument is allowed per slot.
#
DC_SUBSYSTEM
# UBVI 60  1    ( 60V V/I Source in Universal Backplane 1 : slot 14)
#   SRC    2
# UBVI 60  3    ( 60V V/I Source in Universal Backplane 1 : slot 15)
#   HCU    4
# UBVI 60  6    ( 60V V/I Source in Universal Backplane 1 : slot 16)
#   HCU    7
#   HCU    8
#   HCU    9
# UBVI 60 10    ( 60V V/I Source in Universal Backplane 1 : slot 17)
# UBVI 60 11    ( 60V V/I Source in Universal Backplane 1 : slot 18)
# UBVI 60 12    ( 60V V/I Source in Universal Backplane 1 : slot 19)
# UBVI 60 13    ( 60V V/I Source in Universal Backplane 1 : slot 20)
# DATABITS 1 - 48

# UB_MATRIX
#
# Testhead 1
# XPTs    UB Cage  Slot      Type
# 1-4     1       2        APU
# 5-8     1       3        APU
# 9-12    1       4        APU
# 13-16   1       5        APU
# 17-20   1       6        APU
# 21-24   1       7        APU
# 25-28   1       8        APU
# 29-32   1       9        APU
# 33-36   1      10        APU
# 37-40   1      11        APU
# 41-44   1      12        APU
# 45-48   1      13        APU
END

```

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