



Worldwide Semiconductor Equipment Sales and Service

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Teradyne A585 Mixed Signal Test System

```
#
# Confsim file created on: 04/19/05 22:12:12
#
# A585 tester
# Terabus is present
#   Board ID      879-700-03
#   Serial number
#

ADV_MIXSIG_TH 1
BACKPLANE A
CONFIGID 879-959-02
#Slot Type          Num      XptA XptB Name
  2  000-000-00    0      # 5   6   EMPTY
  3  879-858-25    0      # 7   8   PLFS  CC
  4  879-858-35    0      # 9  10   PLFD  CC
  5  879-853-01    0      # 11  12   HF DIG CC
  6  879-909-00    0      # 13  14   SCC MSTR
  7  879-857-01    0      # 15  16   PMM  CC-01
  8  879-792-00    0      # 17  18   TIME  CC
 14  000-000-00    0      # 19  20   EMPTY
 15  879-858-25    0      # 21  22   PLFS  CC
 16  000-000-00    0      # 23  24   EMPTY
 17  879-906-04    0      # 25  26   VHFAWG CC
 18  000-000-00    0      # 27  28   EMPTY
 19  949-326-10    0      # 29  30   UHFSRC CC
 20  000-000-00    0      # 31  32   EMPTY
 21  000-000-00    0      # 33  34   EMPTY
 22  000-000-00    0      # 35  36   EMPTY
  1  879-656-00    0      # 0   0   RDC48
 12  879-652-00    0      # 3   3   HUC
  9  879-653-00    0      # 0   0   HAC
 10  879-654-00    0      # 0   0   TACH
 11  879-667-00    0      # 0   0   ADV_LINEAR CAL
 13  879-834-01    0      # 0   0   Analog Data Buffer AL
END
```

```
#
# Up to 4 Precision AC Card Cages are allowed
#
PRECISION_AC 1
#Slot Type          Num      Name
  1  879-765-04    0      # PLFDIG
  2  000-000-00    0      # EMPTY
  3  879-764-01    0      # PLFSRC
  4  879-745-20    0      # SMEM
  5  879-764-01    0      # PLFSRC
  6  879-745-20    0      # SMEM
  7  000-000-00    0      # EMPTY
  8  879-781-00    0      # PACS CAGE INT
END
```

Ref # 0642-3
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Teradyne A585 Mixed Signal Test System (continued)

```
PRECISION_AC 2
#Slot Type           Num      Name
  1  879-772-01      0      # HFDIG
  2  879-742-20      0      # CMEM
  3  000-000-00      0      # EMPTY
  4  000-000-00      0      # EMPTY
  5  879-780-00      0      # VHFAWG
  6  000-000-00      0      # EMPTY
  7  000-000-00      0      # EMPTY
  8  879-781-00      0      # PACS CAGE INT
END
```

```
HSD50_CHAN_CAGE 1
#Slot Type           Num      Name
  1  879-933-50      0      # H50 DMF
  2  879-933-50      0      # H50 DMF
  3  879-933-50      0      # H50 DMF
  4  879-933-50      0      # H50 DMF
  5  879-934-01      0      # H50 MFS
  6  879-933-50      0      # H50 DMF
  7  879-933-50      0      # H50 DMF
  8  879-933-50      0      # H50 DMF
  9  879-933-50      0      # H50 DMF
END
```

```
HSD50_CHAN_CAGE 2
#Slot Type           Num      Name
  1  879-933-50      0      # H50 DMF
  2  879-933-50      0      # H50 DMF
  3  879-933-50      0      # H50 DMF
  4  879-933-50      0      # H50 DMF
  5  879-934-01      0      # H50 MFS
  6  879-933-50      0      # H50 DMF
  7  879-933-50      0      # H50 DMF
  8  879-933-50      0      # H50 DMF
  9  879-933-50      0      # H50 DMF
END
```

```
HSD50_SEQ_CAGE 1
#Slot Type           Num      Name
  2  879-945-01      0      # H50 AFO
  4  879-942-05      0      # H50 SFO
  5  879-934-01      0      # H50 MFS
  6  879-937-02      0      # H50 SCM
  7  879-938-01      0      # H50 DMC
  8  879-937-02      0      # H50 SCM
END
```

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Teradyne A585 Mixed Signal Test System (continued)

```
ADV_MIXSIG_TH 1
BACKPLANE B
CONFIGID 879-941-01
#Slot Type Num Name
23 879-935-50 0 # H50 DTH
24 879-935-50 0 # H50 DTH
25 879-935-50 0 # H50 DTH
26 879-935-50 0 # H50 DTH
27 879-935-50 0 # H50 DTH
28 879-935-50 0 # H50 DTH
29 879-935-00 0 # H50 DTH
30 879-935-50 0 # H50 DTH
31 879-936-00 0 # H50 THS
32 879-935-00 0 # H50 DTH
33 879-935-50 0 # H50 DTH
34 879-935-50 0 # H50 DTH
35 879-935-50 0 # H50 DTH
38 879-943-01 0 # H50 TDR
40 879-935-00 0 # H50 DTH
41 879-935-50 0 # H50 DTH
42 879-935-00 0 # H50 DTH
43 879-935-50 0 # H50 DTH
44 879-936-00 0 # H50 THS
END
```

```
HSD50_DIG_SIG_CAGE 1
#Slot Type Num Name
1 879-953-00 0 # VBF
2 879-939-01 0 # DSI
3 879-745-00 0 # S_MEM
4 879-957-00 0 # DCB
5 879-742-40 0 # C_MEM
6 879-745-00 0 # S_MEM
7 879-957-00 0 # DCB
8 879-742-40 0 # C_MEM
9 879-731-00 0 # CAGE INTR
END
```

```
#
# Trigger Switch Yard
#
# Note: The logical slot numbers below correspond to the physical slot
# numbers only for test systems which contain a TSY card
# cage. In test systems which contain an SCS/TSY card cage the
# mapping is:
#
# Logical TSY slot (below) Physical slot
# 1 -> 2
# 3 -> 1
#
```

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```
TSY CAGE
#Slot Type          Num      Name
  1  879-655-01    0      # TSY
  2  000-000-00    0      # EMPTY
  3  000-000-00    0      # EMPTY
  4  879-671-00    0      # T_DELAY
END

#
# Time Subsystem
#
TIME_SUBSYSTEM
#   Board ID      Name
      879-793-00  # TMS Timer
      879-794-01  # TMS Counter
      879-795-01  # TMS Support
END

#
# UHF Subsection - up to 4 UHF cages are allowed
#
UHF_CARD_CAGE 1
#Slot MotherBoard  Module1      Module2      Mod_Inst_num  Name
01     949-306-00
12/13  949-300-00  949-321-00  949-322-00    # UHF #1
14/15  949-300-00  949-323-00  949-324-00    # UHF #1
END

#
# DC Subsystem -
#
#   MAX_DC_XPT <NUM>          [1 - 192]
#   DC_XPT <NUM>              [1 - 192]
#   DC_XPT <NUM> to <NUM>     [1 - 192]
#   DC_XPT <NUM> - <NUM>      [1 - 192]
#   APU <NUM>                 [1 - 192]
#   APU <NUM> to <NUM>         [1 - 192]
#   APU <NUM> - <NUM>         [1 - 192]
#   SRC <NUM>                 [1 - 13]
#   (sources 1-5 are MATRIX sources 1-5
#     sources 6-13 are DUT sources 1-8)
#   HCU <NUM>                 *[1 - 4]
#   REF HCU <NUM>             *[1 - 4]
#   HVSRC <NUM>               *[1 - 4]
#   PWSRC <NUM>               [1 - 4]
#   DATABITS <NUM> - <NUM>    [1 - 192]
#
# ** These instruments share the same nine-slot cage -- only one
#    instrument is allowed per slot.
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```



Teradyne A585 Mixed Signal Test System (continued)

```
DC_SUBSYSTEM
DC_XPT 1 - 48
SRC 1
SRC 2
SRC 3
SRC 4
REF HCU 5
SRC 6
SRC 7
SRC 8
HCU 9
DATABITS 1 - 48
END
```

```
#
# Array Processor -
# Legal Types : MC860 array processor
# Legal Sizes : 2, 4, and 16MB
#
ARRAY_PROCESSOR
#      Type           Size
      MC860           4MB
END
```

```
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```